substrate including at least any one of a copper region, a copper based region and a copper alloy region, said method comprising the steps of:

removing metal contaminations from said surface and simultaneously carrying out an anti-corrosion treatment by exposing said surface of said semiconductor substrate to a solution containing an anti-corrosive agent; and

C3 Cont'd

subsequently, separately forming a copper-diffusion stopper insulating film over said surface of said semiconductor substrate.

--64. (new) The method as claimed in claim 63, wherein said semiconductor substrate has at least one interconnection made of a metal selected from the group consisting of copper, copper-based materials, and copper alloys, said method further comprising the step of carrying out a chemical mechanical polishing process for forming said at least one interconnection in at least one groove in said semiconductor substrate prior to said removing metal contaminations step.--

REMARKS

Claims 1-33 and 57-62 were previously pending in the application. Claims 4, 6, 20 and 22 are cancelled and new claims 63 and 64 are added. Therefore, claims 1-3, 5, 7-19, 21, 23-33 and 57-64 are presented for consideration.

Claims 1-4, 6, 16-20, 22, 32, 33 and 57-62 are rejected as unpatentable over AVANZINO et al. 6,350,687.

Reconsideration and allowance are respectfully requested because the reference does not disclose or suggest the step of removing metal contaminations from a surface and simultaneously or subsequently carrying out an anti-corrosion treatment by exposing the surface to a solution containing an anti-corrosive agent as recited in claims 1 and 18 of the present application.

By way of example, page 30, lines 6-12 disclose a cleaning process that is carried out for removing metal contaminations from the surface of the semiconductor wafer using a carboxylic based cleaning solution such as an oxalic acid solution. The semiconductor wafer is rotated with a supply of cleaning solution to remove CuOx from the surface of the semiconductor wafer.

AVANZINO et al. disclose on column 5, lines 12-20, for example, that oxidation can be prevented on an exposed surface of a copper interconnection or copper alloy interconnection by the formation of a passivating layer on the interconnection after the chemical mechanical polishing process. AVANZINO et al. at column 5, lines 43-47, further disclose that by using the passivating film, the formation of all copper oxide film is avoided.

AVANZINO et al. do not disclose a need for removing any oxidation formed by the chemical mechanical polishing process. Specifically, column 6, lines 44-48 of AVANZINO et al. disclose that a further cleaning step removes contaminants such as

abrasives, electrolytes, and copper compounds from the surface of the wafer. The copper compounds are waste copper from the CMP process, not copper oxide formed during the CMP process.

As the reference does not disclose that which is recited, the anticipation rejection is not viable. Accordingly, reconsideration and allowance of claims 1 and 18 are respectfully requested. Claims 2-17, 19-33 and 57-62 depend from claims 1 or 18 respectively and further define the invention and are also believed patentable over the cited prior art.

As noted in the Official Action, page 3, lines 1-3 of the present application disclose removing metal contaminations from a surface of the semiconductor wafer using a carboxylic based cleaning solution.

MPEP §2143.01 states that the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990).

The disclosed prior art teaches removing oxidation using a carboxylic based cleaning solution. AVANZINO et al. teach a method of avoiding the formation of all copper oxide film by using a passivating film. Accordingly, the methods taught by applicants' disclosed prior art and AVANZINO et al. are alternative methods of avoiding the formation of copper oxide film. Therefore, one having ordinary skill in the art would not

be motivated to combine the two teachings to render obvious claims 1 and 18 of the present application.

New claim 63 recites removing metal contaminations from a surface of a semiconductor substrate and simultaneously carrying out an anti-corrosion treatment. The Official Action indicates column 6, lines 36-65 of AVANZINO et al. for providing support for an anti-corrosion treatment carried out at the same time as a cleaning process. This assertion is not supported by the reference.

Specifically, column 6, lines 44-48 of AVANZINO et al. disclose that subsequent to CMP procedures a further cleaning step can be conducted to remove contaminants. Column 6, lines 50-52 of AVANZINO et al. disclose that the cleaned surface 30 is treated to form a controlled passivating film prior to any substantial oxidation. Accordingly, AVANZINO et al. teach a CMP procedure followed possibly by a cleaning step to remove contaminants and then a subsequent step of forming a controlled passivating film (carrying out an anti-corrosion treatment).

AVANZINO et al. do not disclose or suggest removing metal contaminations from the surface and simultaneously carrying out an anti-corrosion treatment as recited in claim 63. Claim 64 depends from claim 63 and further defines the invention and is also believed patentable over the cited prior art.

In view of the present amendment and the foregoing remarks, it is believed that the present application has been

placed in condition for allowance. Reconsideration and allowance are respectfully requested.

Attached hereto is a marked-up version showing the changes made to the claims. The attached page is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

Respectfully submitted,

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"VERSION WITH MARKINGS TO SHOW CHANGES MADE"

IN THE CLAIMS:

Claim 1 has been amended as follows:

--1. (twice amended) A method of treating a surface of a semiconductor substrate, said surface of said semiconductor substrate including at least any one of a copper region, a copper based region and a copper alloy region, said method comprising the steps of:

removing metal contaminations from said surface and simultaneously or subsequently carrying out an anti-corrosion treatment by exposing said surface of said semiconductor substrate to a solution containing an anti-corrosive agent; and

subsequently, separately forming a copper-diffusion stopper insulating film over said surface of said semiconductor substrate.--

Claim 18 has been amended as follows:

--18. (twice amended) A method of forming a semiconductor substrate having at least an interconnection made of a metal selected from the group consisting of copper, copper based materials, and copper alloys, said method comprising the steps of:

carrying out a chemical mechanical polishing process for forming said at least interconnection in at least a groove in said semiconductor substrate;

subsequently removing metal contaminations from a surface of said semiconductor substrate and simultaneously or subsequently carrying out an anti-corrosion treatment by exposing [a] said surface of said semiconductor substrate to a solution containing an anti-corrosive agent; and

subsequently, separately forming a copper-diffusion stopper insulating film over said surface of said semiconductor substrate.--